Amendments to the Claims

The following listing of claims replaces all prior versions and listings of claims:

1-24. (Cancelled).

25. (Currently amended) Apparatus for receiving and unpadding, successively received, padded blocks of data, each of the padded blocks of data including a first number of data bits that the apparatus initially receives serially in a serial data signal, and each of the padded blocks being converted by the apparatus to an unpadded block that includes a second number of data bits that is less than the first number, the apparatus comprising:

means for deriving from a single reference clock signal first and second further clock signals having respective, different, first and second frequencies~~, the first frequency being suitable for use of~~;

means for using the first further clock signal ~~in at least some processing of the padded blocks, and the second frequency being suitable for use of~~ to assemble in parallel from the serial data signal a group of successive data bits equal in number to the first number without regard for where in the group padding bits occur; and

means for using the second further clock signal ~~in at least some processing of the unpadded blocks~~ to separate from successive ones of the groups successive unpadded blocks and to output each of said unpadded blocks in parallel.

26. (Currently amended) The apparatus defined in claim 25 wherein the padded blocks are received by the apparatus one after another at ~~the~~ a predetermined rate, ~~each padded block being received serially,~~ and wherein the apparatus further comprises:

means for outputting unpadded blocks at the predetermined rate.

27. (Original) The apparatus defined in claim 26 further comprising:

means for registering each successive padded block.

28. (Currently amended) The apparatus defined in claim 27 wherein the means for registering is at least partly controlled by the ~~first~~ second further clock signal.

29. (Original) The apparatus defined in claim 28 further comprising:

means for removing padding from each padded block registered by the means for registering to produce a corresponding unpadded block.

30. (Original) The apparatus defined in claim 29 further comprising:

means for converting each unpadded block to a plurality of successive sub-blocks.

31. (Original) The apparatus defined in claim 30 wherein the means for converting is at least partly controlled by the second further clock signal.

32. (Original) The apparatus defined in claim 25 wherein each padded block consists of 66 bits

of data, and each unpadded block consists of 64 bits of data.

33. (Currently amended) The apparatus defined claim 25 wherein the means for deriving comprises:

first frequency dividing circuitry for dividing frequency of a common signal by a first division factor to produce the second further clock signal, the common signal ~~coming~~ being derived from but having a different frequency than the reference clock signal.

34. (original) The apparatus defined in claim 33 wherein the means for deriving further comprises:

second frequency dividing circuitry for dividing the frequency of the common signal by a second division factor to produce the first further clock signal.

35. (Currently amended) The apparatus defined in claim 33 wherein the means for deriving further comprises:

frequency multiplying circuitry for multiplying frequency of a signal ~~coming~~ being derived from but having a different frequency than the reference clock signal to produce the common signal.

36. (Original) The apparatus defined in claim 35 wherein the means for deriving further comprises:

frequency pre-division circuitry for dividing frequency of the reference clock signal by a

pre-division factor to produce the signal operated on by the frequency multiplying circuitry.

37. (Original) The apparatus defined in claim 26 wherein the reference clock signal has a reference frequency having an integer-based relationship to the predetermined rate.

38. (Original) The apparatus defined in claim 37 wherein the means for deriving comprises:

means for performing integer-based manipulation of the reference frequency to produce the first and second further clock signals.

39. (Original) The apparatus defined in claim 38 wherein the means for performing comprises:

first means for performing first integer-based manipulation of the reference frequency to produce a common signal; and

second means for performing second integer-based frequency manipulation of the common signal to produce the second further clock signal.

40. (Original) The apparatus defined in claim 39 wherein the means for performing further comprises:

third means for performing third integer-based frequency manipulation of the common signal to produce the first further clock signal.

41. (Currently amended) The apparatus defined in claim 25 ~~further comprising~~ wherein the means for using the second further clock signal comprises:

byte alignment circuitry for using the padding of the padded blocks to locate data block boundaries.

42-46. (Cancelled)

47. (Currently amended) A method of receiving and unpadding, successively received, padded blocks of data, each of the padded blocks of data including a first number of data bits that are initially received serially in a serial data signal, and each of the padded blocks being converted by the method to an unpadded block that includes a second number of data bits that is less than the first number, the method comprising:

deriving from a reference clock signal a common signal;

producing first and second further clock signals from the common signal;

using the first further clock signal in at least some processing of the padded data, including using the first further clock signal to assemble in parallel from the serial data signal a group of successive data bits equal in number to the first number without regard for where in the group padding bits occur; and

using the second further clock signal in at least some processing of the unpadded data, including using the second further clock signal to separate from successive ones of the groups successive unpadded blocks and to output each of said unpadded blocks in parallel, wherein the first and second further clock signals have respective, different, first

and second frequencies, at least one of which is different from frequency of the common signal.

48. (Original) The method defined in claim 47 wherein the common signal frequency is different from frequency of the reference signal.

49. (Original) The method defined in claim 47 wherein the first and second frequencies are both different from the common signal frequency.

50. (Original) The method defined in claim 47 wherein the deriving comprises:

using integer-based frequency manipulation of the reference clock signal to produce the common signal.

51. (Original) The method defined in claim 47 wherein the producing comprises:

using integer-based frequency manipulation of the common signal to produce at least one of the first and second further clock signals.

52-56. (Cancelled).

57. (Currently amended) Apparatus for receiving and unpadding, successively received, padded blocks of data, each of the padded blocks of data including a first number of data bits that the apparatus initially receives serially in a serial data signal, and each of the padded blocks being converted by the apparatus to an unpadded block that includes a second number of data bits that in less than the first number, the apparatus comprising:

first circuitry adapted to derive from a reference clock signal a common signal;

second circuitry adapted to produce first and second further clock signals from the common signal;

third circuitry adapted to use the first further clock signal in at least some processing of the padded data, including using the first further clock signal to assemble in parallel from the serial data signal a group of successive data bits equal in number to the first number without regard for where in the group padding bits occur; and

fourth circuitry adapted to use the second further clock signal in at least some processing of the unpadded data, including using the second further clock signal to separate from successive ones of the groups successive unpadded blocks and to output each of said unpadded blocks in parallel, wherein the first and second further clock signals have respective, different, first and second frequencies, at least one of which is different from frequency of the common signal.

58. (Original) The apparatus defined in claim 57 wherein the common signal frequency is different from frequency of the reference clock signal.

59. (Original) The apparatus defined in claim 57 wherein the first and second frequencies are both different from the common signal frequency.

60. (Original) The apparatus defined in claim 57 wherein the first circuitry comprises:

circuitry for performing integer-based frequency manipulation of the reference clock signal to produce the common signal.

61. (Original) The apparatus defined in claim 60 wherein the second circuitry comprises:

circuitry for performing integer-based frequency manipulation of the reference clock signal to produce the common signal.